

ABSTRACT OF THE DISCLOSURE

A pseudo-NMOS circuit includes a load PFET electrically connected between a power supply and an output node, and an NFET circuit having a plurality of inputs connected between the output node and ground. A feedback PFET is electrically connected between the power supply and the output node, in parallel with the load PFET, and is controlled by a signal at the output node of the pseudo-NMOS circuit.

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